

1           1.    A method comprising:  
2                forming a circuit element over a triple well in a  
3   substrate; and  
4                biasing a well of said triple well through a  
5   resistor.

1           2.    The method of claim 1 including forming an  
2   integrated inductor over a triple well.

1           3.    The method of claim 1 including forming a P-type  
2   well in an N-type well formed in said substrate.

1           4.    The method of claim 3 including biasing the N-  
2   type and P-type wells through different resistors.

1           5.    The method of claim 1 including providing a  
2   common bias potential to different wells through separate  
3   resistors for each well.

1           6.    The method of claim 5 including forming a radio  
2   frequency circuit element over a triple well.

1           7.    The method of claim 5 including biasing said  
2   wells through resistors having a resistance greater than  
3   one hundred ohms.

1           8.    The method of claim 7 including forming a  
2   complementary metal oxide semiconductor transistor over a  
3   triple well and biasing at least one of the wells of said  
4   triple well through a resistor.

1           9.    The method of claim 1 including forming a  
2   plurality of triple wells in said substrate and forming a  
3   circuit element over each of said triple wells, biasing at  
4   least one well of each of said triple wells through a  
5   common potential, each of said potentials being applied to  
6   said wells through a resistor.

1           10.   The method of claim 9 including applying a supply  
2   potential to said plurality of wells through a resistor.

1           11.   An integrated circuit comprising:  
2               a substrate;  
3               a circuit element formed over said substrate;  
4               a triple well formed in said substrate under said  
5   circuit element; and  
6               a resistor connectable to a bias potential and  
7   coupled to a well of said triple well.

1           12.   The circuit of claim 11 wherein the triple well  
2   each includes a P-well formed in an N-well formed in the  
3   substrate.

1           13. The circuit of claim 11 wherein said resistor is  
2 coupled to a supply voltage.

1           14. The circuit of claim 11 including a plurality of  
2 circuit elements formed over said substrate, each of said  
3 circuit elements formed over a triple well, each of said  
4 triple wells having at least one well connectable to a bias  
5 potential.

1           15. The circuit of claim 14 including a resistor  
2 coupled to each of said wells, each of said resistors  
3 connectable to a bias potential so as to supply resistance  
4 in the path of said bias potential to said well.

1           16. The circuit of claim 15 wherein the same  
2 potential is applied to a plurality of wells.

1           17. The circuit of claim 16 wherein said plurality of  
2 resistors are connectable to the same bias source.

1           18. The circuit of claim 17 wherein each of said  
2 resistors is connectable to a supply voltage.

1           19. The circuit of claim 16 wherein each of said  
2 resistors is connected to a path that is common with the  
3 path of each of the other resistors coupled to wells.

1           20. A method comprising:  
2               forming a first circuit element over a triple  
3 well in a substrate;  
4               biasing a first well of said first triple well  
5 through a first resistor with a first bias potential;  
6               forming a second circuit element over a second  
7 triple well in a substrate; and  
8               biasing a second well of said second triple well  
9 through a second resistor coupled to said first bias  
10 potential.

1           21. The method of claim 20 including coupling the  
2 first bias potential to said first and second wells through  
3 a common trace to a supply potential.

1           22. The method of claim 20 including forming an  
2 integrated inductor over the first triple well.

1           23. The method of claim 20 including forming a P-type  
2 well and an N-type well formed in said substrate.

1           24. The method of claim 23 including biasing the N-  
2 type and P-type wells through different resistors.

1           25. The method of claim 20 including forming a radio  
2 frequency element over said first triple well.

1           26. The method of claim 25 including biasing said  
2 wells through resistors having a resistance greater than  
3 100 ohms.

1           27. An integrated circuit comprising:  
2           a substrate;  
3           a first circuit element formed over said  
4 substrate;  
5           a first triple well formed in said substrate  
6 under said first circuit element;  
7           a first resistor connectable to a first bias  
8 potential and coupled to a first well of said first triple  
9 well;  
10          a second circuit element formed over said  
11 substrate;  
12          a second triple well formed in said substrate  
13 under said second circuit element; and  
14          a second resistor connectable to the first bias  
15 potential and coupled to the second well of said second  
16 triple well.

1           28. The circuit of claim 27 wherein said first  
2 circuit element is a complementary metal oxide  
3 semiconductor transistor.

1           29. The integrated circuit of claim 27 wherein said  
2 first circuit element is an integrated inductor.

1           30. The integrated circuit of claim 27 wherein said  
2 first bias potential is a supply voltage.